

- Low $r_{DS(on)}$. . . 5 Ω Typical
- Avalanche Energy . . . 30 mJ
- Eight Power DMOS-Transistor Outputs of 150-mA Continuous Current
- 500-mA Typical Current-Limiting Capability
- Output Clamp Voltage . . . 50 V
- Four Distinct Function Modes
- Low Power Consumption

description

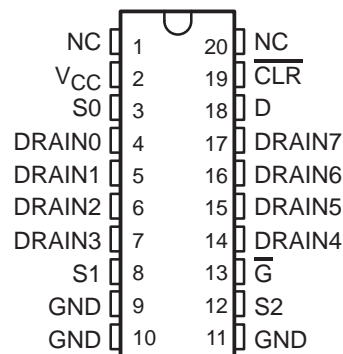
This power logic 8-bit addressable latch controls open-drain DMOS-transistor outputs and is designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and decoders or demultiplexers. This is a multi-functional device capable of storing single-line data in eight addressable latches and 3-to-8 decoder or demultiplexer with active-low DMOS outputs.

Four distinct modes of operation are selectable by controlling the clear (\overline{CLR}) and enable (\overline{G}) inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in (D) terminal is written into the addressed latch. The addressed DMOS-transistor output inverts the data input with all unaddressed DMOS-transistor outputs remaining in their previous states. In the memory mode, all DMOS-transistor outputs remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latch, enable \overline{G} should be held high (inactive) while the address lines are changing. In the 3-to-8 decoding or demultiplexing mode, the addressed output is inverted with respect to the D input and all other outputs are off. In the clear mode, all outputs are off and unaffected by the address and data inputs. When data is low for a given output, the DMOS-transistor output is off. When data is high, the DMOS-transistor output has sink-current capability.

Outputs are low-side, open-drain DMOS transistors with output ratings of 50 V and 150-mA continuous sink-current capability. Each output provides a 500-mA typical current limit at $T_C = 25^\circ\text{C}$. The current limit decreases as the junction temperature increases for additional device protection.

The TPIC6B259 is characterized for operation over the operating case temperature range of -40°C to 125°C .

DW OR N PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

| INPUTS | | | OUTPUT OF ADDRESSED DRAIN | EACH OTHER DRAIN | FUNCTION |
|------------------|----------------|---|---------------------------------|------------------------|-------------------------|
| \overline{CLR} | \overline{G} | D | | | |
| H | L | H | L | Q_{i0} | Addressable Latch |
| H | L | L | H | Q_{i0} | |
| H | H | X | Q_{i0} | Q_{i0} | Memory |
| L | L | H | L | H | 8-Line Demultiplexer |
| L | L | L | H | H | |
| L | H | X | H | H | Clear |

LATCH SELECTION TABLE

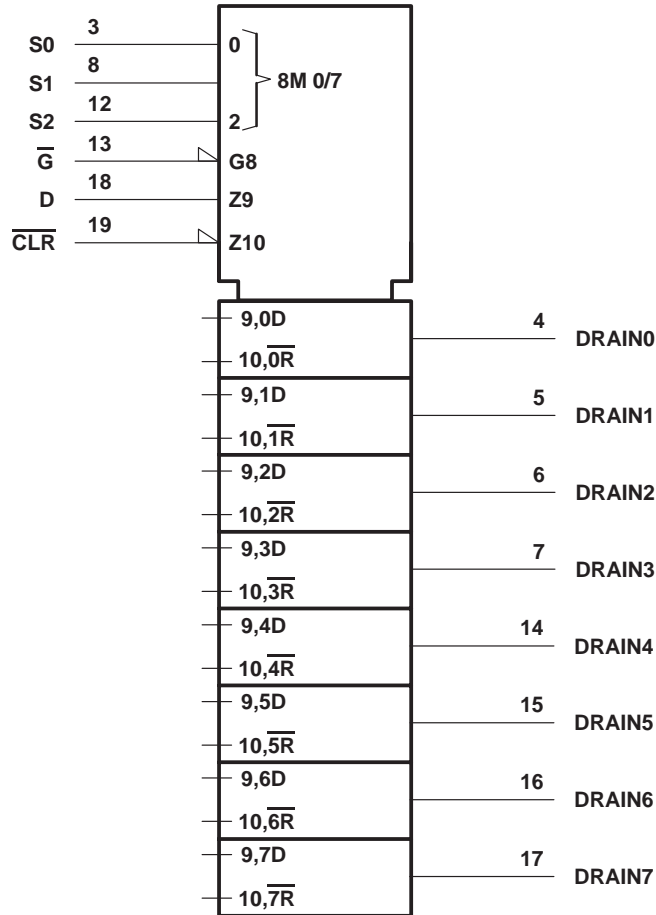
| SELECT INPUTS | | | DRAIN ADDRESSED |
|---------------|----|----|--------------------|
| S2 | S1 | S0 | |
| L | L | L | 0 |
| L | L | H | 1 |
| L | H | L | 2 |
| L | H | H | 3 |
| H | L | L | 4 |
| H | L | H | 5 |
| H | H | L | 6 |
| H | H | H | 7 |

H = high level, L = low level

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logic symbol†

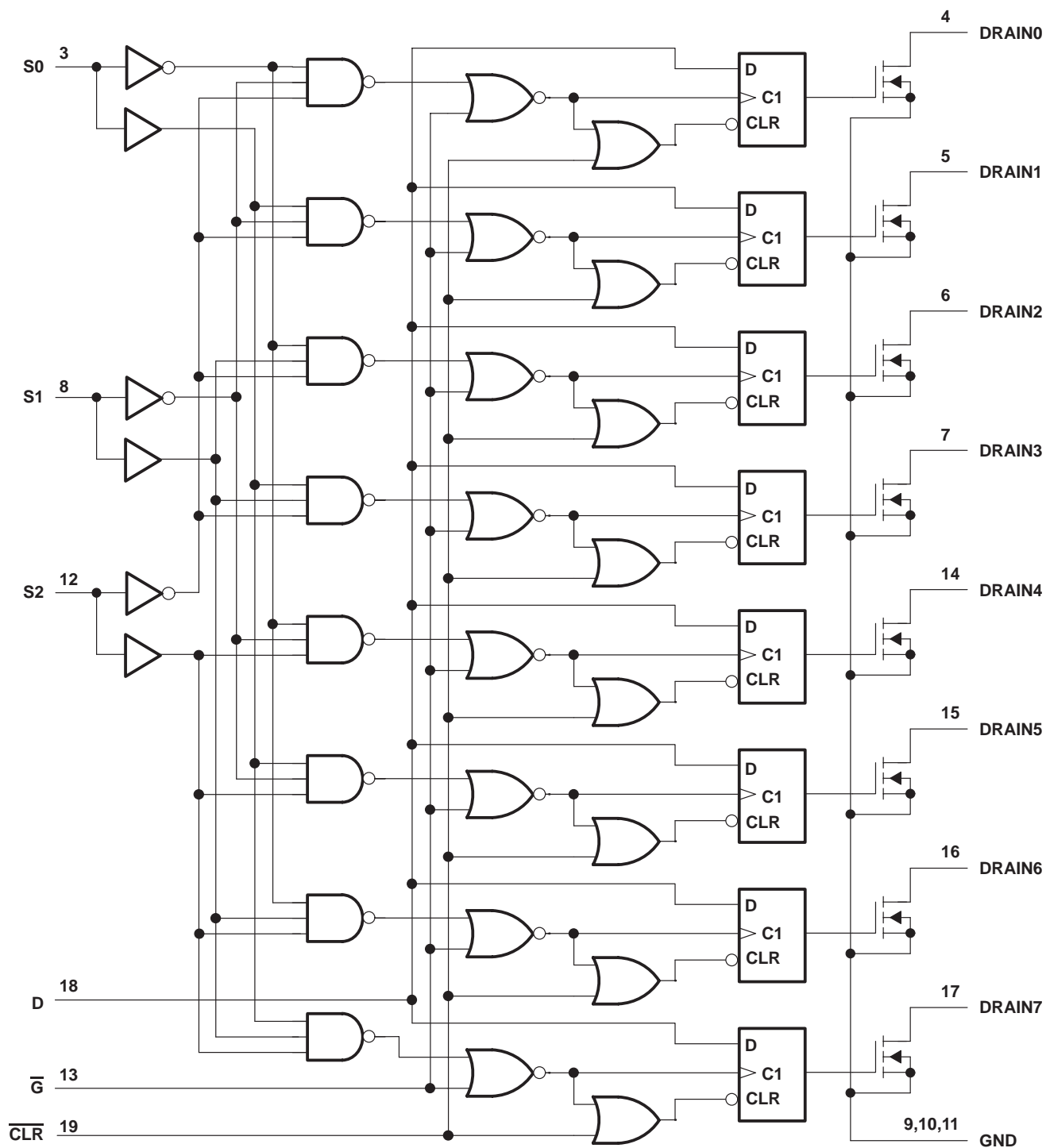


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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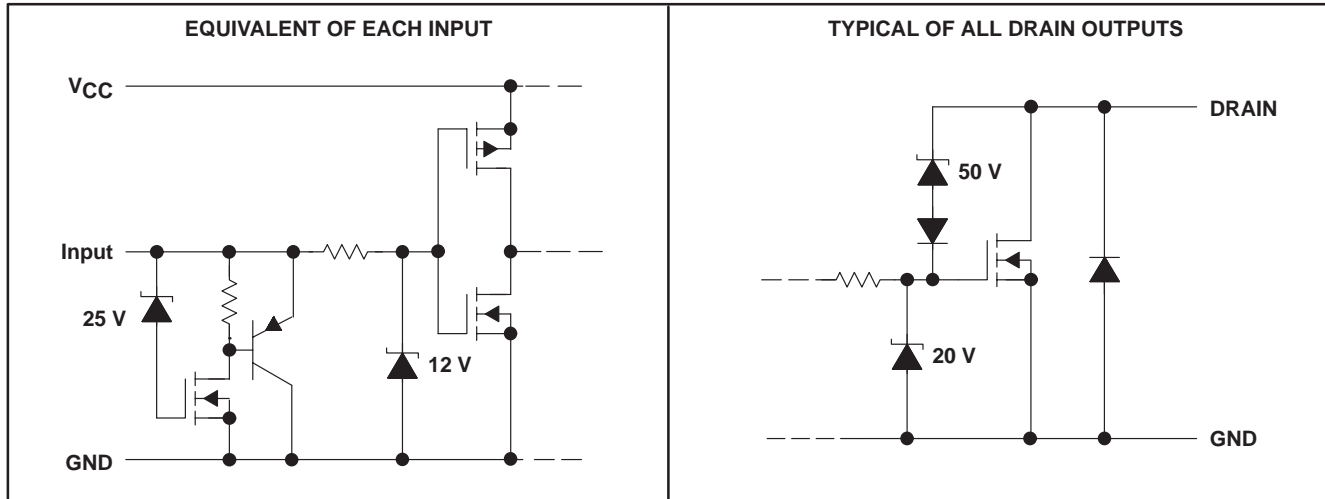
logic diagram (positive logic)



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schematic of inputs and outputs



absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted)†

| | |
|--|------------------------------|
| Logic supply voltage, V_{CC} (see Note 1) | 7 V |
| Logic input voltage range, V_I | -0.3 V to 7 V |
| Power DMOS drain-to-source voltage, V_{DS} (see Note 2) | 50 V |
| Continuous source-to-drain diode anode current | 500 mA |
| Pulsed source-to-drain diode anode current (see Note 3) | 1 A |
| Pulsed drain current, each output, all outputs on, I_D , $T_C = 25^\circ\text{C}$ (see Note 3) | 500 mA |
| Continuous drain current, each output, all outputs on, I_D , $T_C = 25^\circ\text{C}$ | 150 mA |
| Peak drain current single output, I_{DM} , $T_C = 25^\circ\text{C}$ (see Note 3) | 500 mA |
| Single-pulse avalanche energy, E_{AS} (see Figure 4) | 30 mJ |
| Avalanche current, I_{AS} (see Note 4) | 500 mA |
| Continuous total dissipation | See Dissipating Rating Table |
| Operating virtual junction temperature range, T_J | -40°C to 150°C |
| Operating case temperature range, T_C | -40°C to 125°C |
| Storage temperature range | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND.
 2. Each power DMOS source is internally connected to GND.
 3. Pulse duration $\leq 100 \mu\text{s}$ and duty cycle $\leq 2\%$.
 4. DRAIN supply voltage = 15 V, starting junction temperature (T_{JS}) = 25°C, $L = 200 \text{ mH}$, $I_{AS} = 0.5 \text{ A}$ (see Figure 4).

DISSIPATION RATING TABLE

| PACKAGE | $T_C \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR ABOVE $T_C = 25^\circ\text{C}$ | $T_C = 125^\circ\text{C}$ POWER RATING |
|---------|---|---|---|
| DW | 1389 mW | 11.1 mW/°C | 278 mW |
| N | 1050 mW | 10.5 mW/°C | 263 mW |

recommended operating conditions

| | MIN | MAX | UNIT |
|---|---------------|-----|------------------|
| Logic supply voltage, V_{CC} | 4.5 | 5.5 | V |
| High-level input voltage, V_{IH} | 0.85 V_{CC} | | V |
| Low-level input voltage, V_{IL} | 0.15 V_{CC} | | V |
| Pulsed drain output current, $T_C = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$ (see Notes 3 and 5) | -500 | 500 | mA |
| Setup time, D high before $\overline{G}\uparrow$, t_{SU} (see Figure 2) | 20 | | ns |
| Hold time, D high after $\overline{G}\uparrow$, t_H (see Figure 2) | 20 | | ns |
| Pulse duration, t_W (see Figure 2) | 40 | | ns |
| Operating case temperature, T_C | -40 | 125 | $^\circ\text{C}$ |

electrical characteristics, $V_{CC} = 5\text{ V}$, $T_C = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|--|------|-----|---------------|
| $V_{(BR)DSX}$ Drain-to-source breakdown voltage | $I_D = 1\text{ mA}$ | 50 | | | V |
| V_{SD} Source-to-drain diode forward voltage | $I_F = 100\text{ mA}$ | | 0.85 | 1 | V |
| I_{IH} High-level input current | $V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ | | | 1 | μA |
| I_{IL} Low-level input current | $V_{CC} = 5.5\text{ V}$, $V_I = 0$ | | | -1 | μA |
| I_{CC} Logic supply current | $V_{CC} = 5.5\text{ V}$ | All outputs off | 20 | 100 | μA |
| | | All outputs on | 150 | 300 | |
| I_N Nominal current | $V_{DS(on)} = 0.5\text{ V}$, $I_N = I_D$, $T_C = 85^\circ\text{C}$, See Notes 5, 6, and 7 | | 90 | | mA |
| I_{DSX} Off-state drain current | $V_{DS} = 40\text{ V}$, $V_{CC} = 5.5\text{ V}$ | | 0.1 | 5 | μA |
| | $V_{DS} = 40\text{ V}$, $V_{CC} = 5.5\text{ V}$, $T_C = 125^\circ\text{C}$ | | 0.15 | 8 | |
| $r_{DS(on)}$ Static drain-to-source on-state resistance | $I_D = 100\text{ mA}$, $V_{CC} = 4.5\text{ V}$ | See Notes 5 and 6 and Figures 6 and 7 | 4.2 | 5.7 | Ω |
| | $I_D = 100\text{ mA}$, $V_{CC} = 4.5\text{ V}$, $T_C = 125^\circ\text{C}$ | | 6.8 | 9.5 | |
| | $I_D = 350\text{ mA}$, $V_{CC} = 4.5\text{ V}$ | | 5.5 | 8 | |

switching characteristics, $V_{CC} = 5\text{ V}$, $T_C = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----|-----|-----|------|
| t_{PLH} Propagation delay time, low-to-high-level output from D | $C_L = 30\text{ pF}$, $I_D = 100\text{ mA}$, See Figures 1, 2, and 8 | | 150 | | ns |
| t_{PHL} Propagation delay time, high-to-low-level output from D | | | 90 | | ns |
| t_r Rise time, drain output | | | 200 | | ns |
| t_f Fall time, drain output | | | 200 | | ns |
| t_a Reverse-recovery-current rise time | $I_F = 100\text{ mA}$, $di/dt = 20\text{ A}/\mu\text{s}$, See Notes 5 and 6 and Figure 3 | | 100 | | ns |
| t_{rr} Reverse-recovery time | | | 300 | | |

- NOTES: 3. Pulse duration $\leq 100\ \mu\text{s}$ and duty cycle $\leq 2\%$.
 5. Technique should limit $T_J - T_C$ to 10°C maximum.
 6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
 7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at $T_C = 85^\circ\text{C}$.

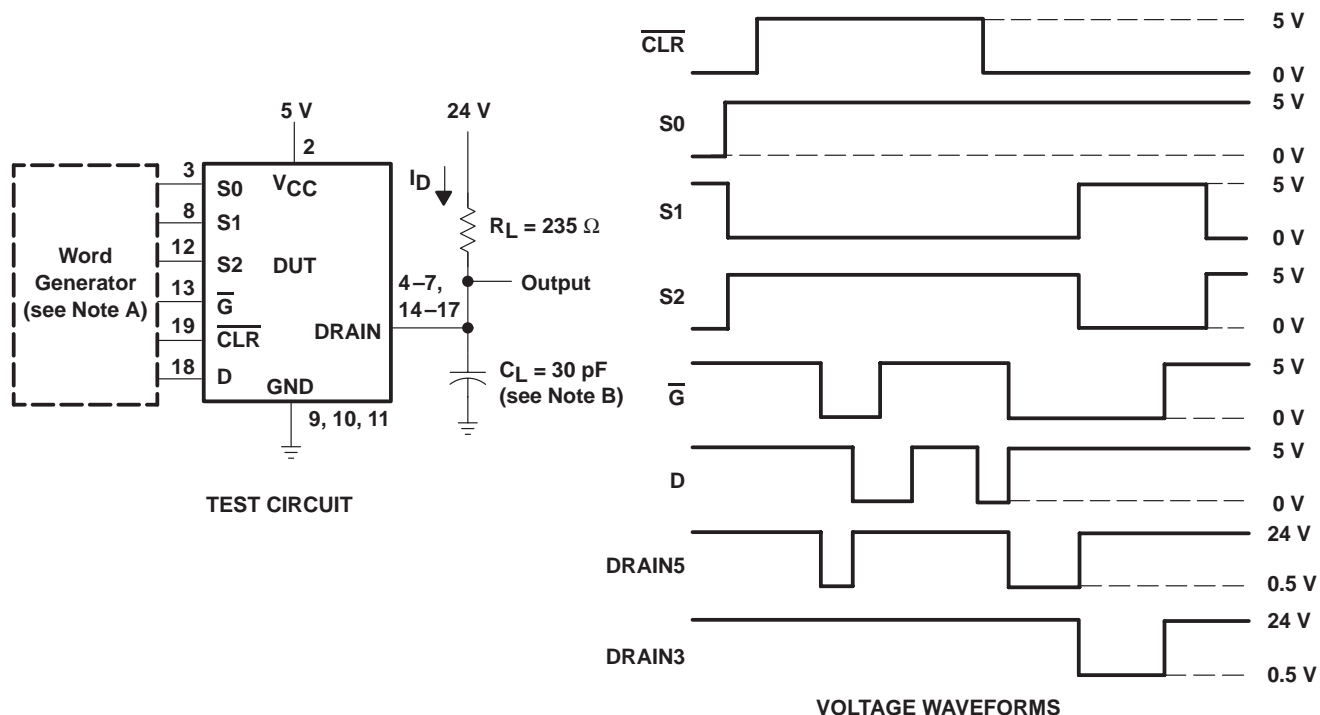
TPIC6B259 POWER LOGIC 8-BIT ADDRESSABLE LATCH

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thermal resistance

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|--|-----------------|--------------------------------|-----|------|
| R _{θJA} | Thermal resistance junction-to-ambient | DW package | | 90 | °C/W |
| | | N package | All 8 outputs with equal power | 95 | |

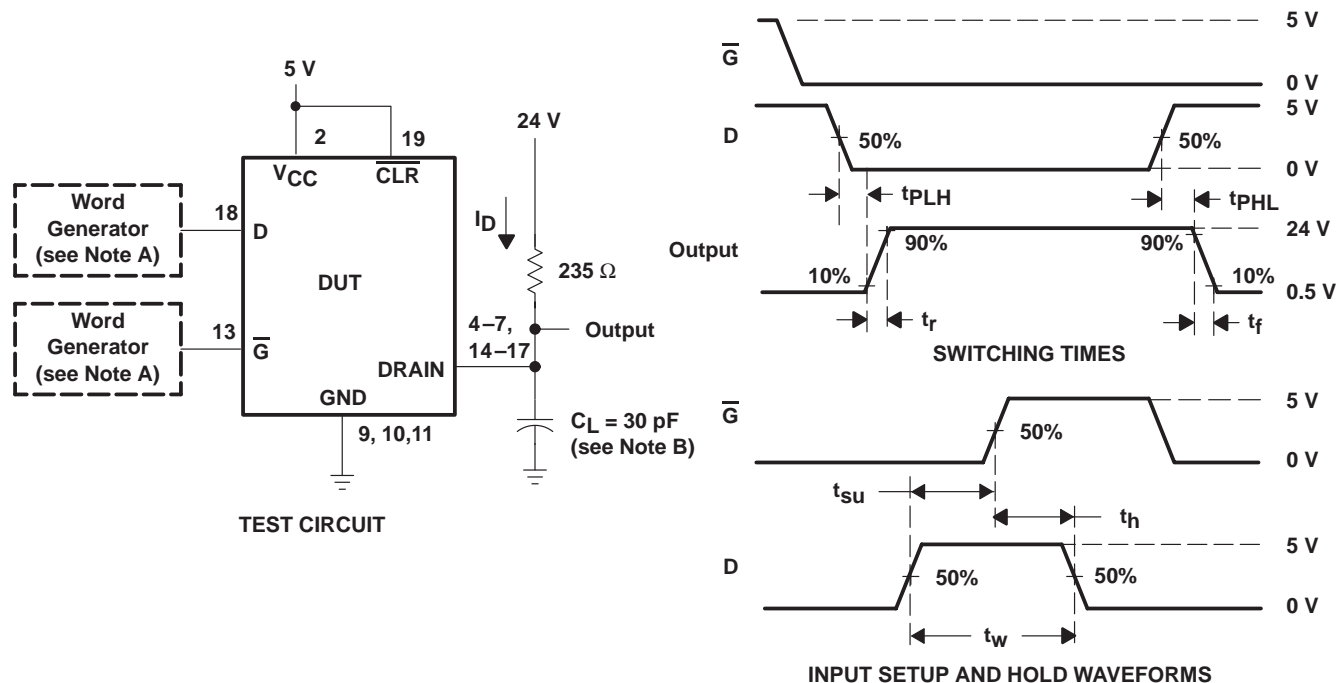
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_O = 50$ Ω.
B. C_L includes probe and jig capacitance.

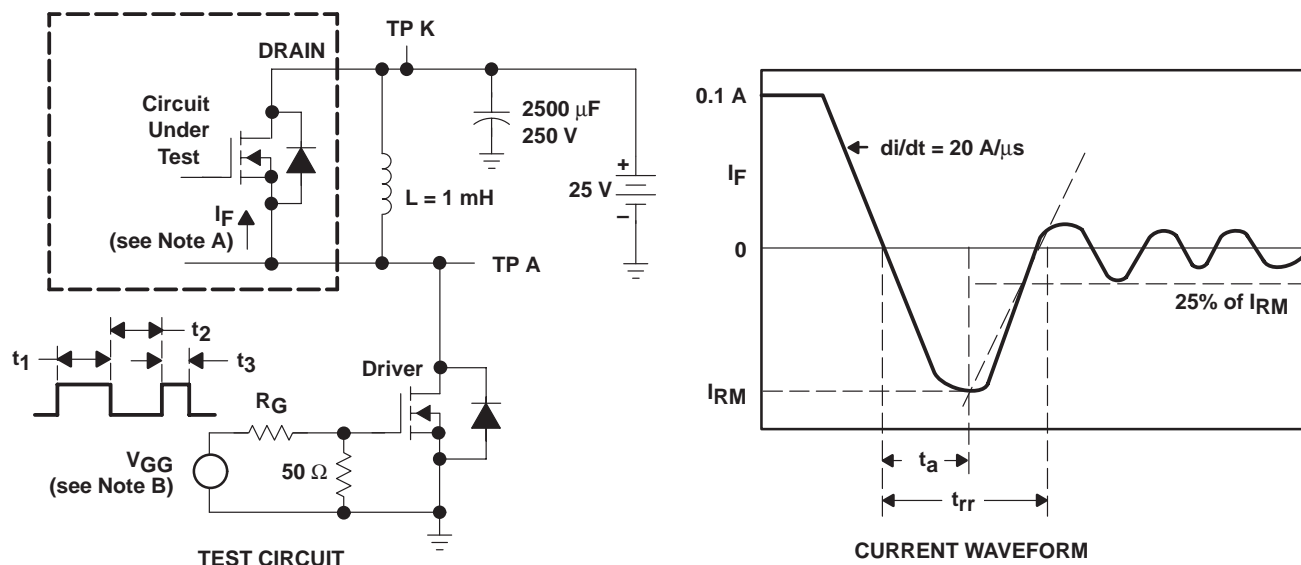
Figure 1. Resistive-Load Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, pulsed repetition rate (PRR) = 5 kHz, $Z_0 = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit, Switching Times, and Voltage Waveforms



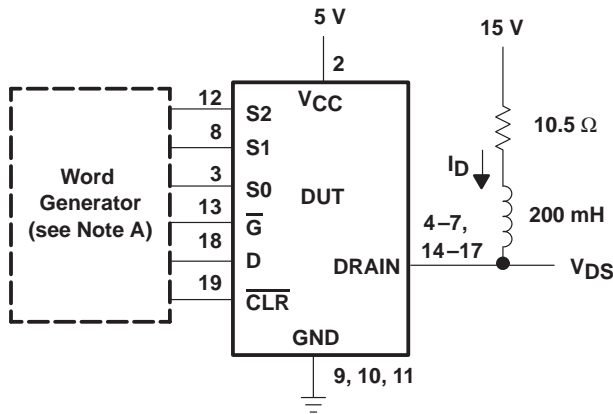
NOTES: A. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.
B. The V_{GG} amplitude and R_G are adjusted for $di/dt = 20$ A/ μ s. A V_{GG} double-pulse train is used to set $I_F = 0.1$ A, where $t_1 = 10 \mu$ s, $t_2 = 7 \mu$ s, and $t_3 = 3 \mu$ s.

Figure 3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-to-Drain Diode

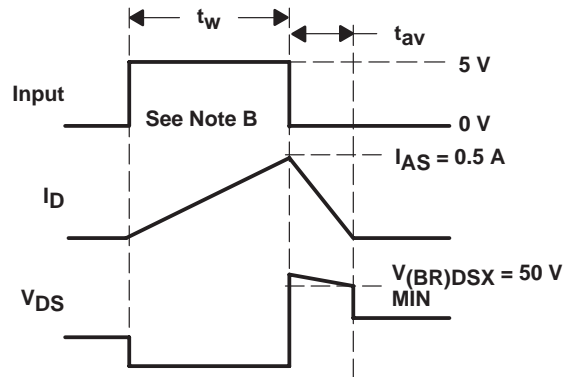
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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

- NOTES: A. The word generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.
 B. Input pulse duration, t_w , is increased until peak current $I_{AS} = 0.5$ A.
 Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2 = 30$ mJ.

Figure 4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

TYPICAL CHARACTERISTICS

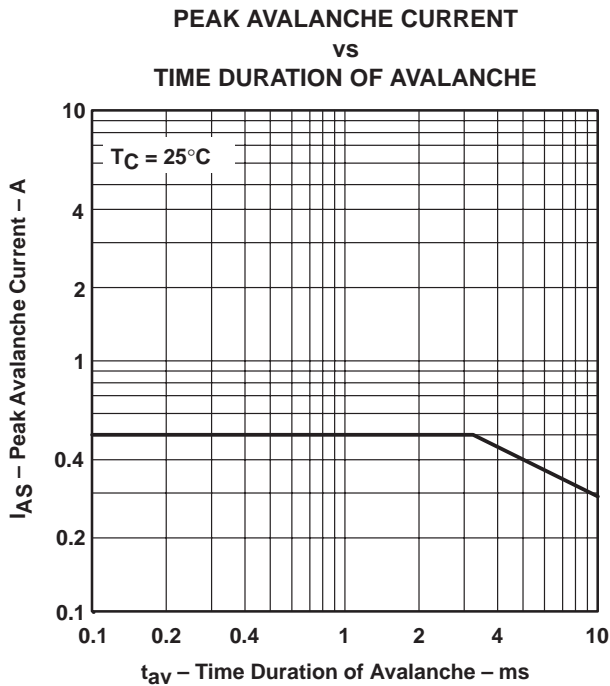
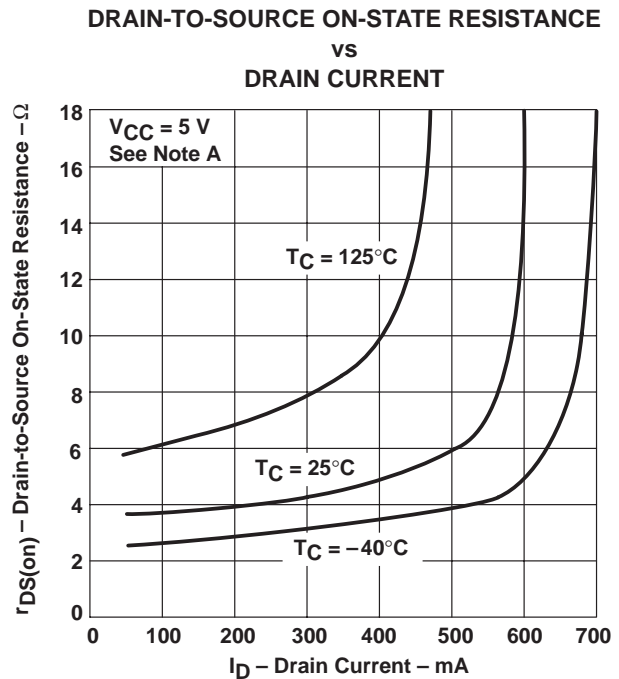


Figure 5



NOTE C: Technique should limit $T_J - T_C$ to 10°C maximum.

Figure 6

TYPICAL CHARACTERISTICS

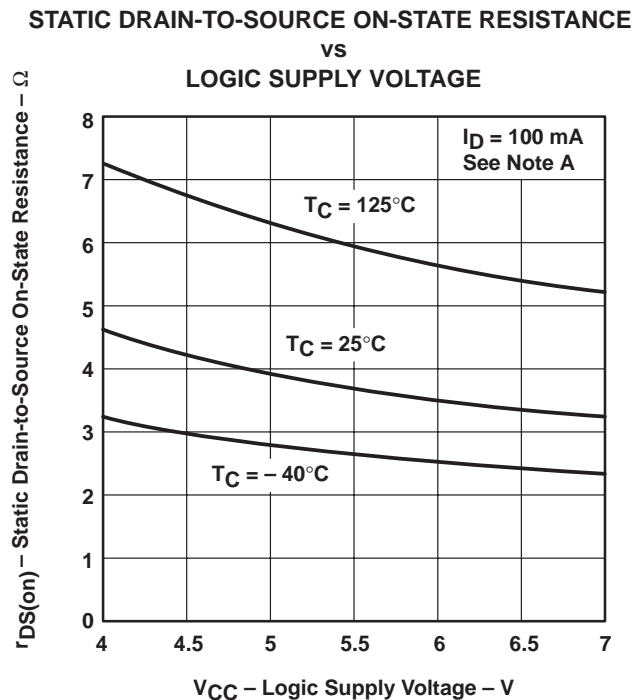


Figure 7

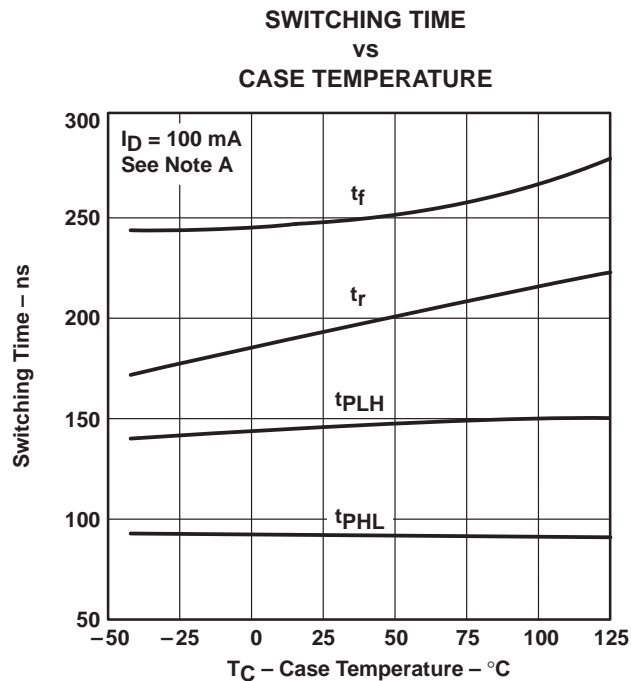


Figure 8

NOTE D: Technique should limit $T_J - T_C$ to 10°C maximum.

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THERMAL INFORMATION

MAXIMUM CONTINUOUS
DRAIN CURRENT OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

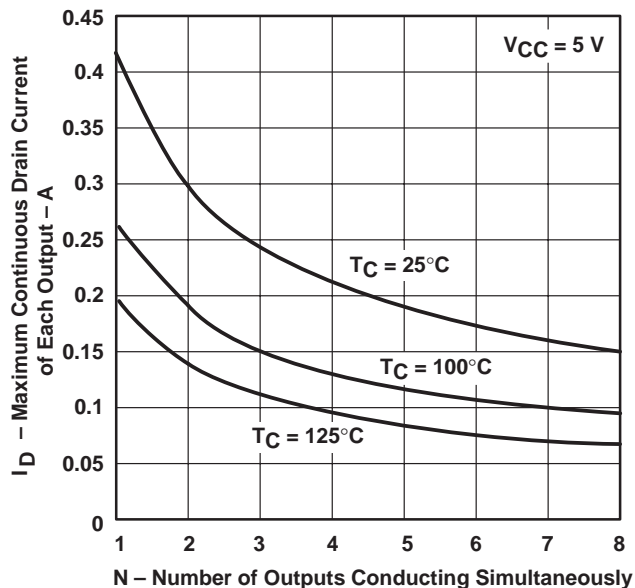


Figure 9

MAXIMUM PEAK DRAIN CURRENT
OF EACH OUTPUT
vs
NUMBER OF OUTPUTS CONDUCTING
SIMULTANEOUSLY

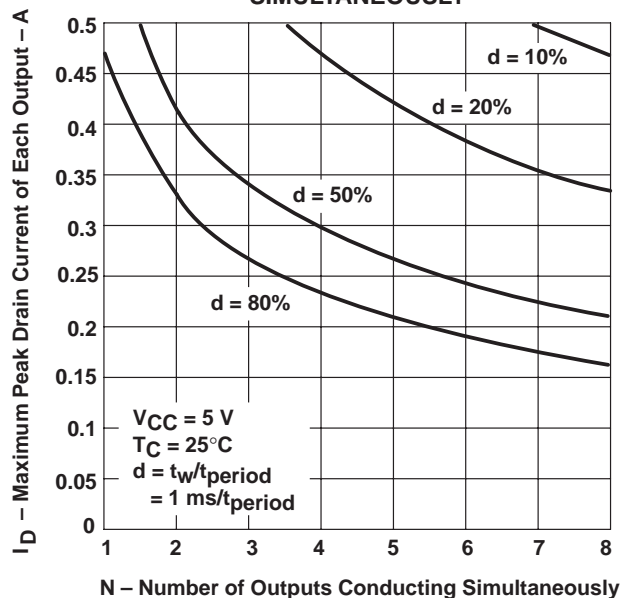


Figure 10

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TPIC6B259DW | ACTIVE | SOIC | DW | 20 | 25 | TBD | CU NIPDAU | Level-1-220C-UNLIM |
| TPIC6B259DWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPIC6B259DWR | ACTIVE | SOIC | DW | 20 | 2000 | TBD | CU NIPDAU | Level-1-220C-UNLIM |
| TPIC6B259DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPIC6B259N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

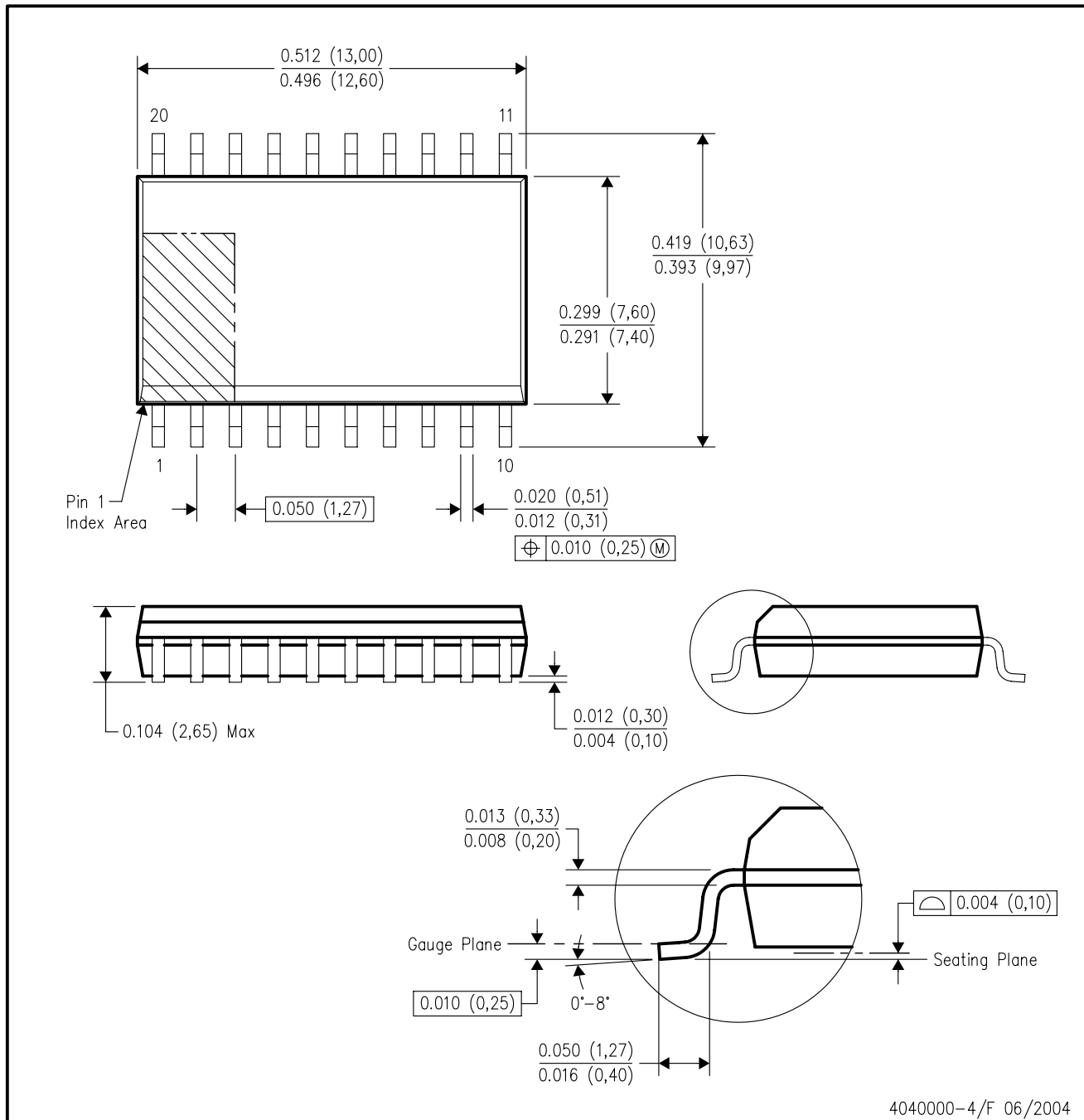
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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